WHAT IS CLAIMED IS:

1. A method of fabricating a transistor, comprising:

forming a gate structure outwardly of a semiconductor substrate, wherein the gate structure comprises a gate, a gate insulator and sidewalls;

forming source region and a drain region in the substrate using the gate structure as a mask, wherein a channel is defined in the substrate between the source region and the drain region; and

forming a bottomwall/sidewall junction capacitance reduction region extending within and between the source region and the drain region, wherein the bottomwall/sidewall junction capacitance reduction region extends at least partially through the bottomwall junction or the sidewall junction.

2. The method of Claim 1, wherein a concentration of dopants implanted to form the bottomwall/sidewall junction capacitance reduction region is about $1x10^{12}$ cm^{-2} to $1x10^{14}$ cm^{-2}.

3. The method of Claim 1, wherein the transistor is an n-MOS type transistor and the bottomwall/sidewall junction capacitance reduction region is implanted using energies of about 20-200 kV.

4. The method of Claim 1, wherein the transistor is a p-MOS type transistor and the bottomwall/sidewall junction capacitance reduction region is implanted using energies of about 30-100 kV.

5. The method of Claim 1, wherein a non-encroachment distance is at least about 150 angstroms.

6. The method of Claim 5, wherein at least a portion of the bottomwall/sidewall junction capacitance reduction region is implanted through the gate structure.

7. The method of Claim 1, wherein a dopant concentration of the bottomwall/sidewall junction capacitance reduction region peaks substantially at the bottomwall junction.

8. The method of Claim 1, wherein the bottomwall/sidewall junction capacitance reduction region is formed with the same mask configuration for a complimentary transistor as is used during the formation of the source and drain regions.

9. A transistor, comprising:

a gate structure outwardly of a semiconductor substrate, wherein the gate structure comprises a gate, a gate insulator and sidewalls;

a source region and a drain region in the substrate, wherein the source region and the drain region are formed using the gate structure as a mask;

a channel defined in the substrate inwardly of the gate structure and between the source and drain regions; and

a bottomwall/sidewall junction capacitance reduction region extending within and between the source region and the drain region, wherein the bottomwall/sidewall junction capacitance reduction region extends at least partially through bottomwall junction or the sidewall junction.

10. The transistor of Claim 9, wherein a concentration of dopants implanted to form the bottomwall/sidewall junction capacitance reduction region is about $1x10^{12}$ cm^{-2} to $1x10^{14}$ cm^{-2}.

11. The transistor of Claim 9, wherein the transistor is an n-MOS type transistor and the bottomwall/sidewall junction capacitance reduction region is implanted using energies of about 20-200 kV.

12. The transistor of Claim 9, wherein the transistor is a p-MOS type transistor and the bottomwall/sidewall junction capacitance reduction region is implanted using energies of about 30-100 kV.

13. The transistor of Claim 9, wherein a non-encroachment distance is at least about 150 angstroms.

14. The transistor of Claim 13, wherein at least a portion of the bottomwall/sidewall junction capacitance reduction region is implanted through the gate structure.

15. The transistor of Claim 9, wherein a dopant concentration of the bottomwall/sidewall junction capacitance reduction region peaks substantially at the bottomwall junction.

16. The transistor of Claim 9, wherein the bottomwall/sidewall junction capacitance reduction region is formed with the same mask configuration as is used during the formation of the source and drain regions.

17. An integrated circuit comprising a plurality of metal oxide semiconductor field effect transistors (MOSFET), each MOSFET comprising:

a gate structure outwardly of a semiconductor substrate, wherein the gate structure comprises a gate, a gate insulator and sidewalls;

a source region and a drain region in the substrate, wherein the source region and the drain region are formed using the gate structure as a mask;

a channel defined in the substrate inwardly of the gate structure and between the source and drain regions; and

a bottomwall/sidewall junction capacitance reduction region extending within and between the source region and the drain region, wherein the bottomwall/sidewall junction capacitance reduction region extends at least partially through bottomwall junction or the sidewall junction.

18. The integrated circuit of Claim 17, wherein a concentration of dopants implanted to form the bottomwall/sidewall junction capacitance reduction region of each MOSFET is about $1x10^{12}$ cm^{-2} to $1x10^{14}$ cm^{-2}.

19. The integrated circuit of Claim 17, wherein at least a portion of the bottomwall/sidewall junction capacitance reduction region of each MOSFET is implanted through the gate structure.

20. The integrated circuit of Claim 17, wherein a dopant concentration of the bottomwall/sidewall junction capacitance reduction region of each MOSFET peaks substantially at the bottomwall junction.